REMARKS

This Amendment is supplemental to the Response filed January 21, 2003. Claims 1-17 are active for examination. By this Amendment, claims 4 and 11 are amended to correct clerical errors. No new matter is added.

As indicated in the previous response, the present application claims subject matter patentable over the references of record and is in condition for allowance. Favorable consideration is respectfully requested. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Recognition Under 37 C.F.R. §10.9(b)

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MARK-UP VERSION SHOWING CHANGES MADE

IN THE CLAIMS

Please amend claims 4 and 11 as follows:

4. (Three Times Amended) A semiconductor device comprising a delay locked loop including:

an input buffer receiving an external clock and outputting a first internal clock;

a delay circuit delaying said first internal clock to output a second internal clock;

a detector detecting which of said first and second clocks is advanced in a phase; and

a gray code counter using a gray code, responsive to an output of said detector, for selectively generating one of a signal to increase an amount of delay of said delay circuit and a signal to decrease said amount of delay of said delay circuit;

wherein said output of said detector indicates that said first clock is in advance of said second clock in a phase or said second clock is in advance of said first clock in a phase.

11. (Three Times Amended) A semiconductor device comprising a delay locked loop including:

a first input buffer receiving at least a first external clock and a second external clock complementary in phase to said first external clock, and outputting a first internal clock at the timing of the rising edge of said first external clock when a potential of said first external clock is equal to that of said second external clock;

a second input buffer receiving at least said first and second external clocks, and outputting a second internal clock at the timing of the rising edge of said second external clock when a potential of said first external clock is equal to that of said second external clock;

a first delay circuit delaying said first internal clock to output a third internal clock;

a second delay circuit delaying said second internal clock to output a fourth internal clock;

a detector detecting which of said first and second clocks is advanced in a phase; and

a gray code counter using a gray code, responsive to an output of said detector, for selectively generating one of a signal to increase an amount of delay of said first delay circuit and an amount of delay of said second delay circuit, and a signal to decrease said amount of delay of said first delay circuit and said amount of delay of said second delay circuit;

wherein said output of said detector indicates that said first clock is in advance of said second clock in a phase or said second clock is in advance of said first clock in a phase.